FIG.1

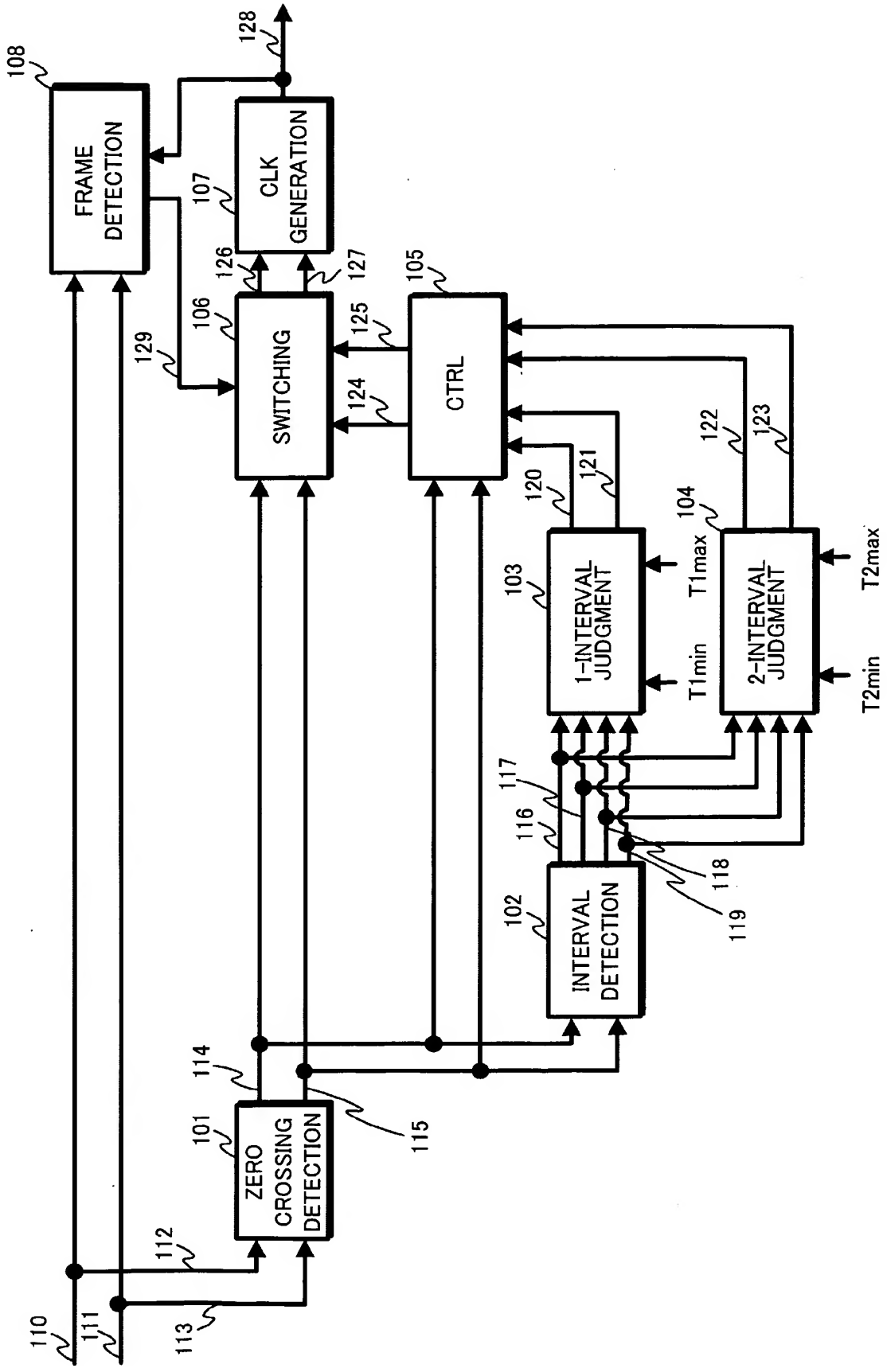

FRAME DETECTION
CLK GENERATION
SWITCHING
CTRL
1-INTERVAL JUDGMENT
2-INTERVAL JUDGMENT
INTERVAL DETECTION
ZERO CROSSING DETECTION
T1max
T1min
T2max
T2min
101
102
103
104
105
106
107
108
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129

FIG. 2

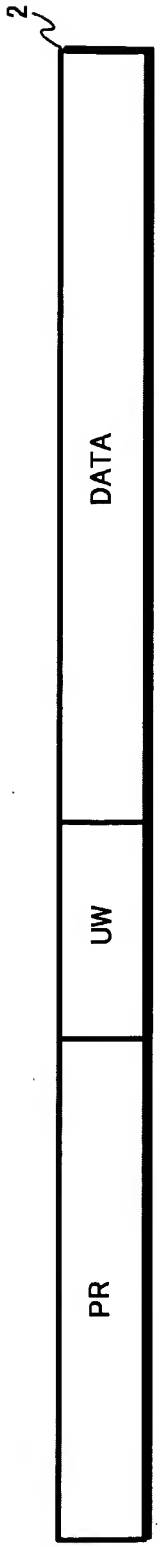


FIG. 3

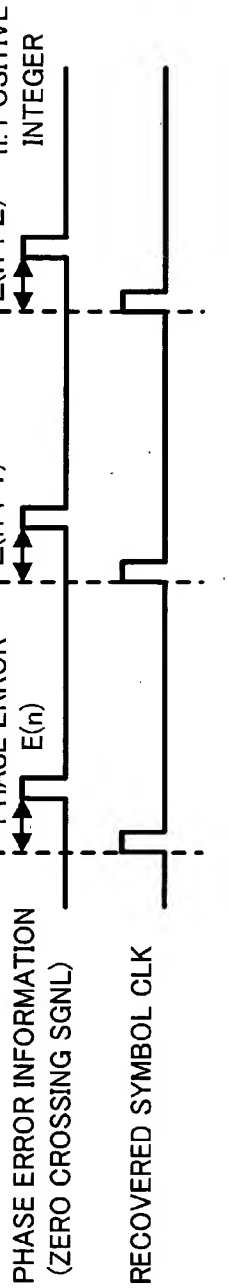

n: POSITIVE INTEGER
E(n+2)
E(n+1)
PHASE ERROR E(n)
PHASE ERROR INFORMATION (ZERO CROSSING SGNL)
RECOVERED SYMBOL CLK

FIG. 4

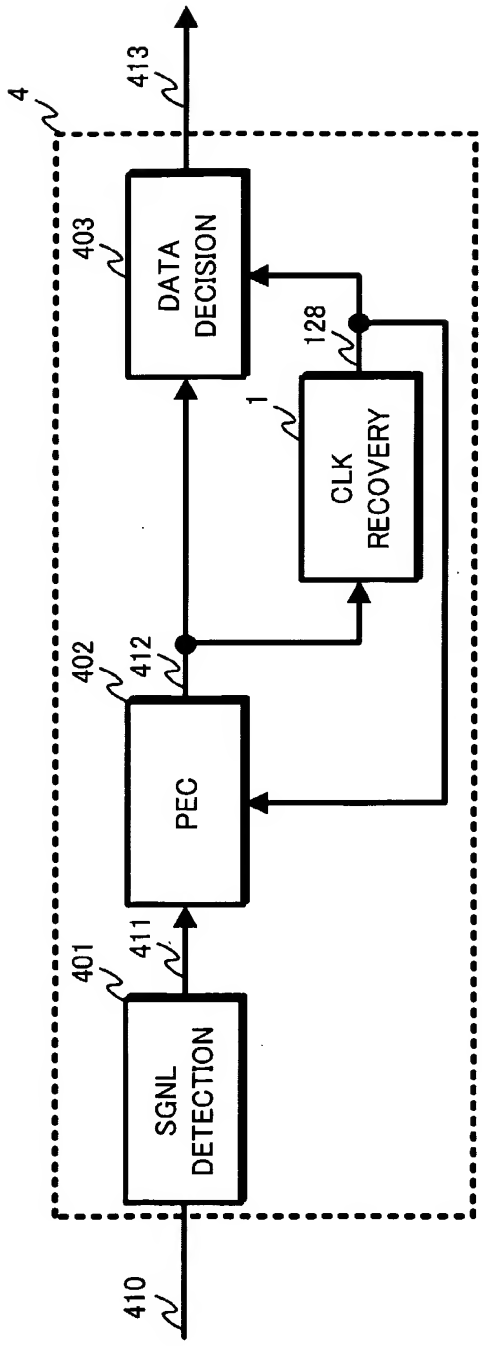

4
413
403
DATA DECISION
128
1
CLK RECOVERY
402
412
PEC
401
411
SGNL DETECTION
410

FIG. 5

BIT X_n X_{n+1}	PHASE TRANSITION
1 1	$-3\pi/4$
0 1	$3\pi/4$
0 0	$\pi/4$
1 0	$-\pi/4$

FIG. 6

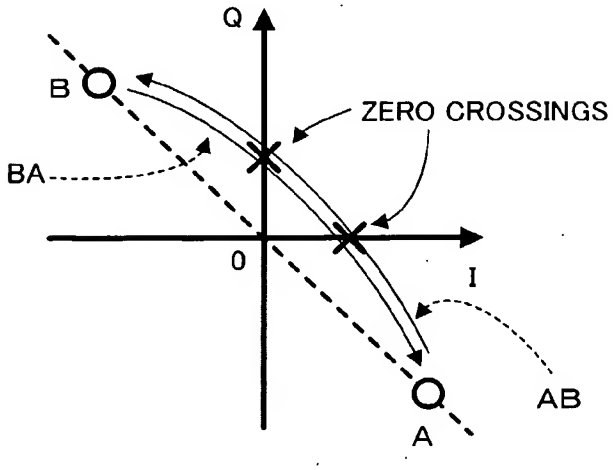


FIG. 7

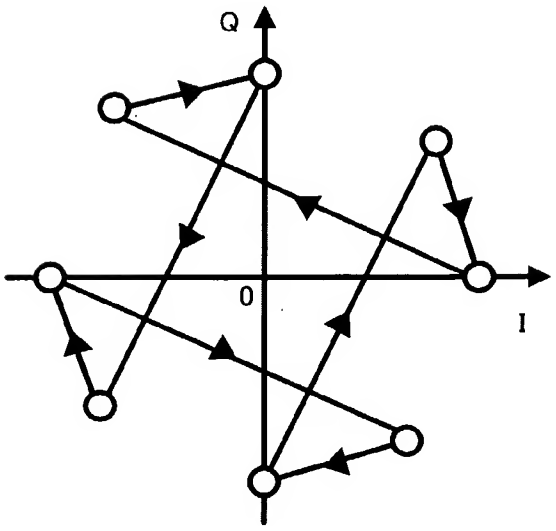


FIG. 8

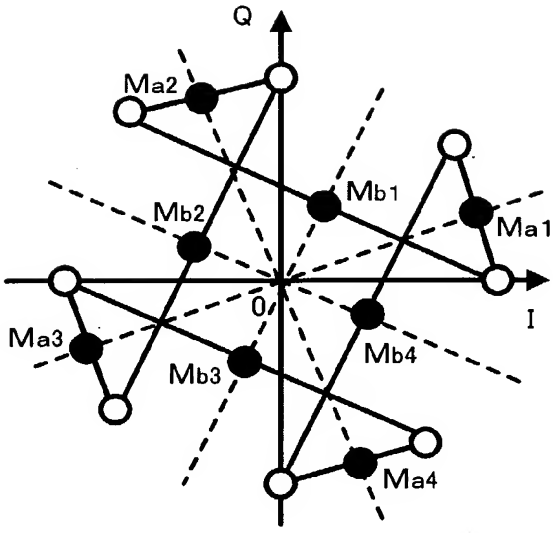


FIG. 9

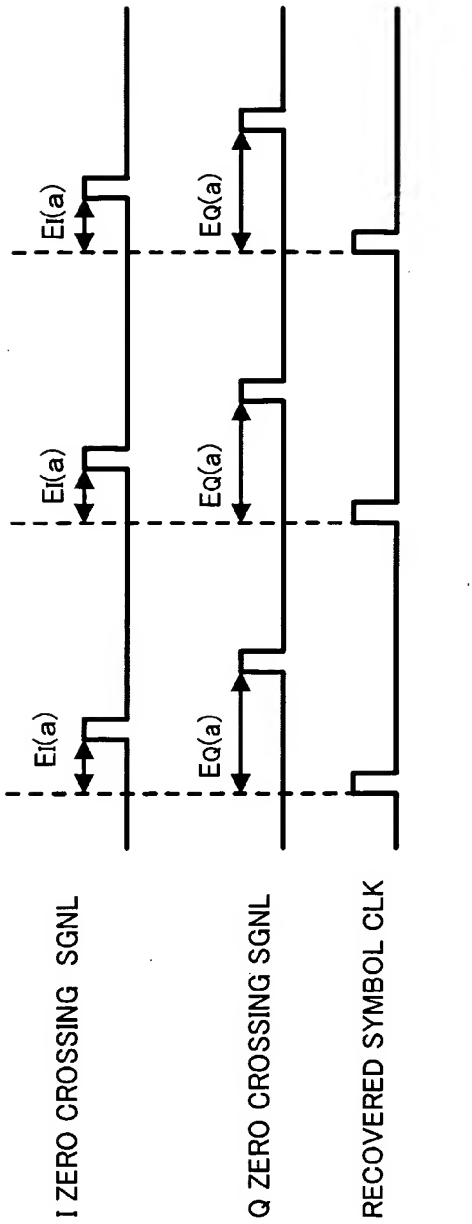

EI(a)
EI(a)
EI(a)
EQ(a)
EQ(a)
EQ(a)
I ZERO CROSSING SGNL
Q ZERO CROSSING SGNL
RECOVERED SYMBOL CLK

FIG. 10

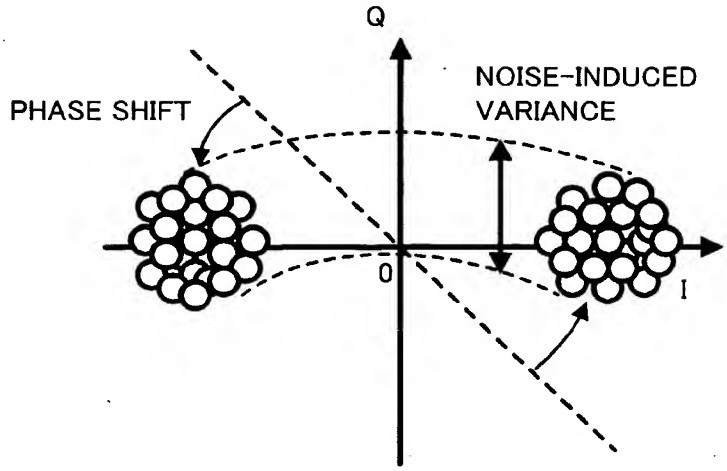

Q
PHASE SHIFT
NOISE-INDUCED
VARIANCE
0
I

FIG. 11

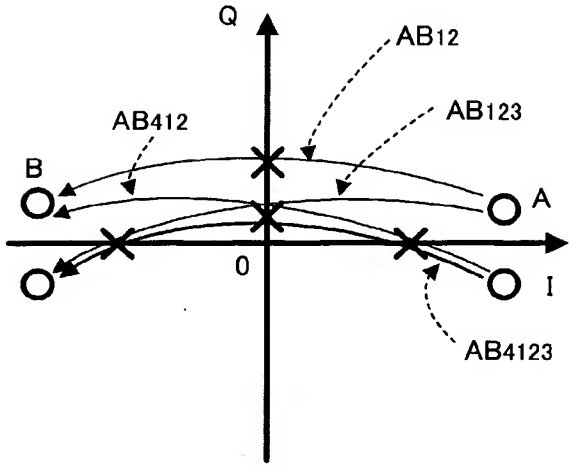

Q
AB12
AB123
AB412
B
A
0
I
AB4123

FIG.12

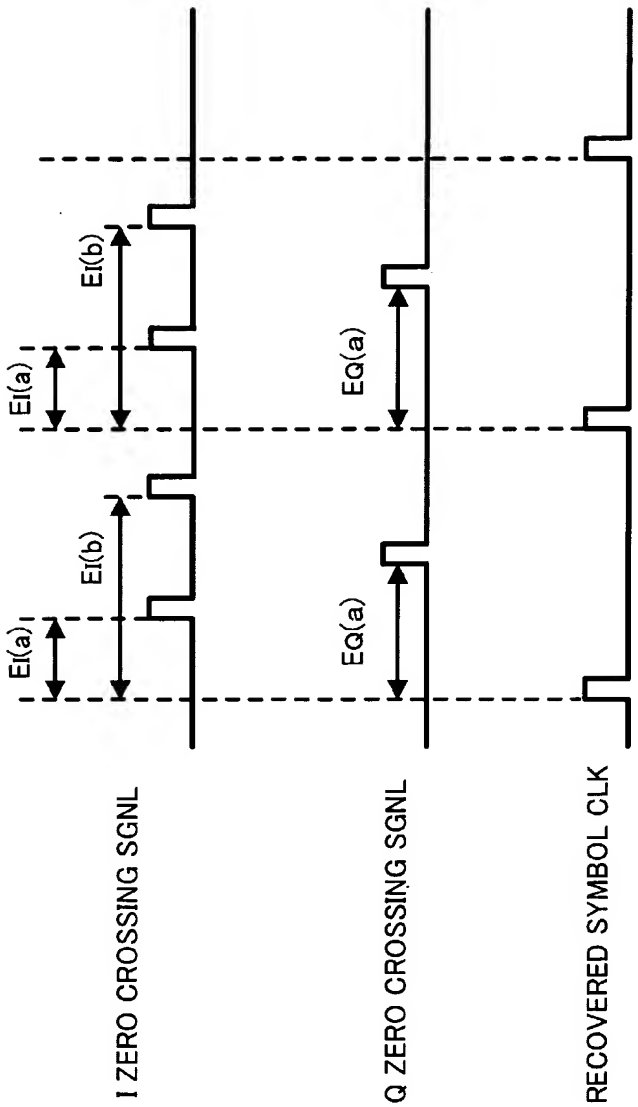

I ZERO CROSSING SGNL
Q ZERO CROSSING SGNL
RECOVERED SYMBOL CLK
EI(a)
EI(b)
EI(a)
EI(b)
EQ(a)
EQ(a)

FIG.13

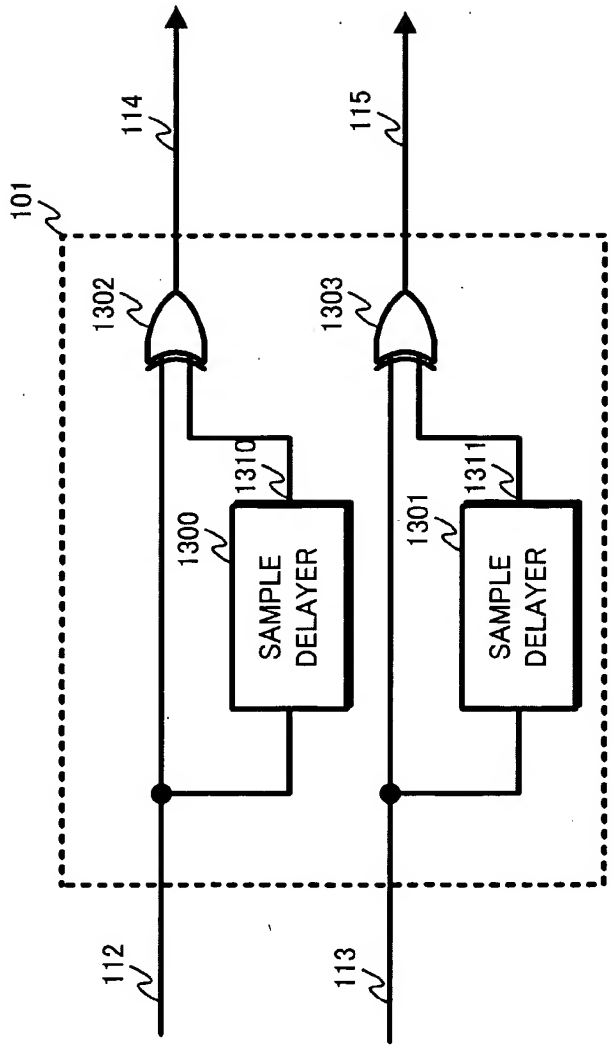

101
114
115
1302
1303
1310
1311
1300
1301
SAMPLE DELAYER
SAMPLE DELAYER
112
113

FIG.14

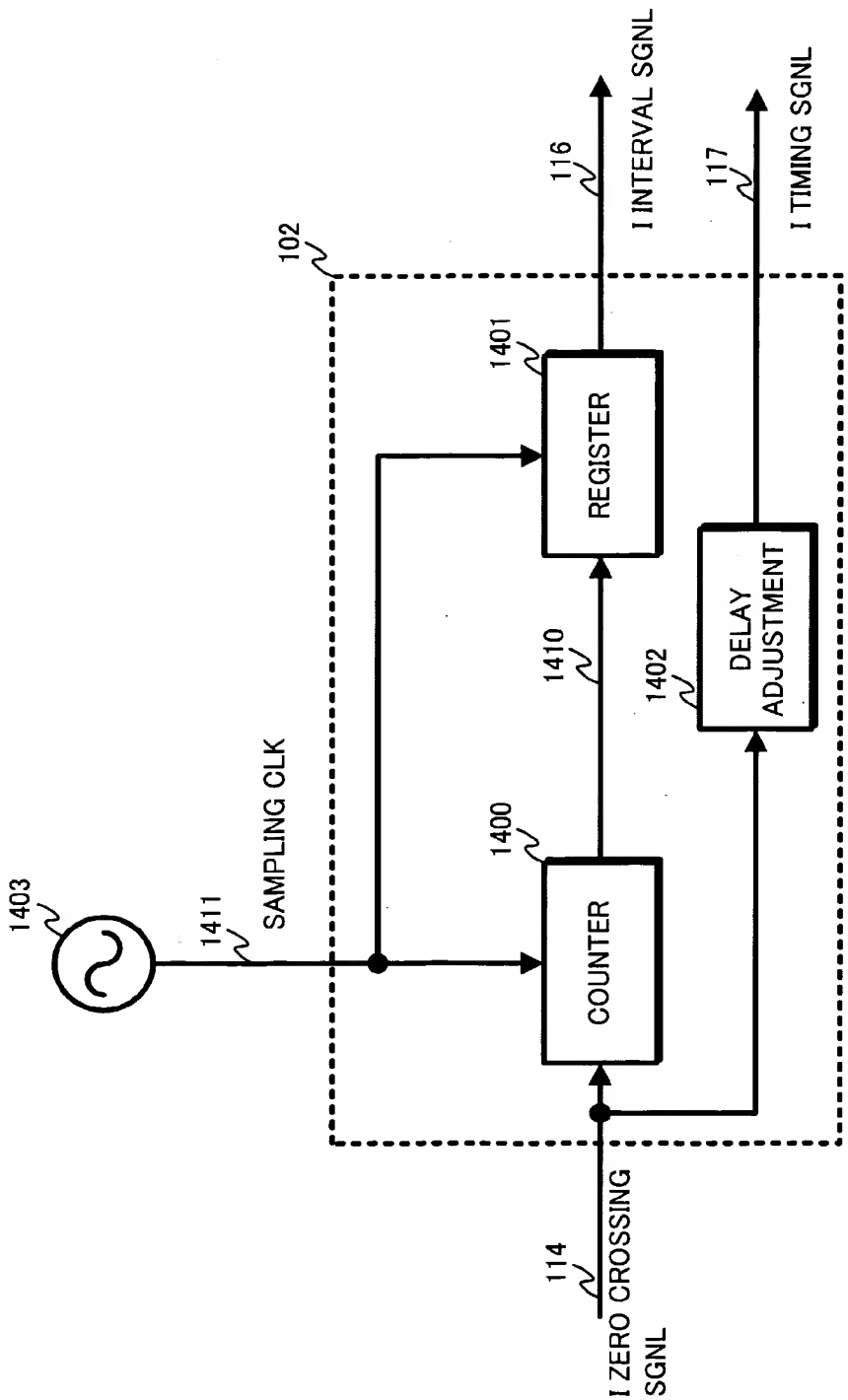

1403
1411
SAMPLING CLK
102
1400
COUNTER
1410
1401
REGISTER
1402
DELAY ADJUSTMENT
116
I INTERVAL SGNL
117
I TIMING SGNL
114
I ZERO CROSSING SGNL

FIG.15

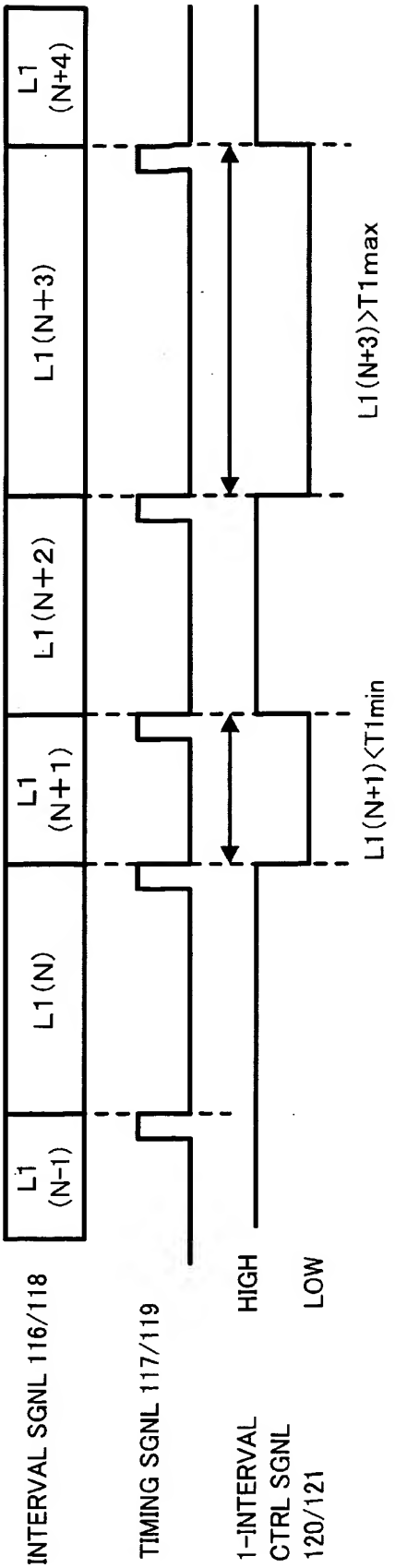

L1 (N-1)
L1 (N)
L1 (N+1)
L1 (N+2)
L1 (N+3)
L1 (N+4)
INTERVAL SGNL 116/118
TIMING SGNL 117/119
1-INTERVAL CTRL SGNL 120/121
HIGH
LOW
L1(N+3)>T1max
L1(N+1)<T1min

FIG.16

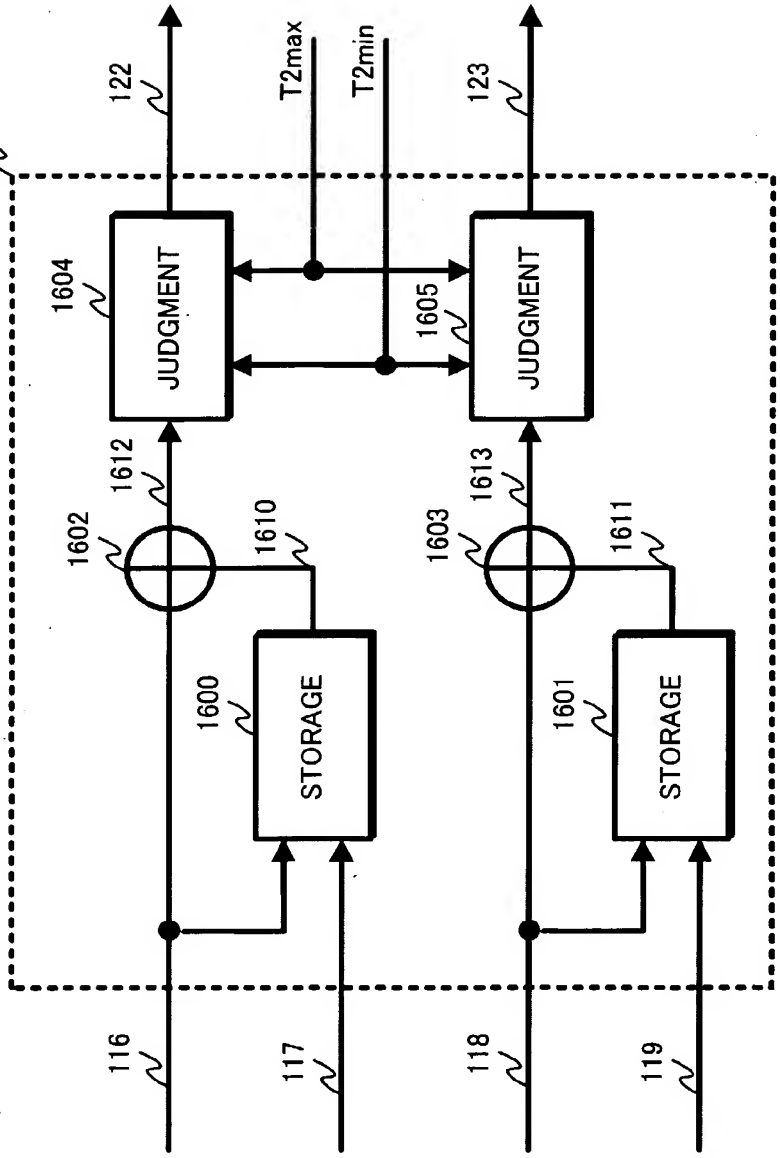

104
122
T2max
T2min
123
1604
JUDGMENT
1605
JUDGMENT
1612
1613
1602
1610
1603
1611
1600
STORAGE
1601
STORAGE
116
117
118
119

FIG.17

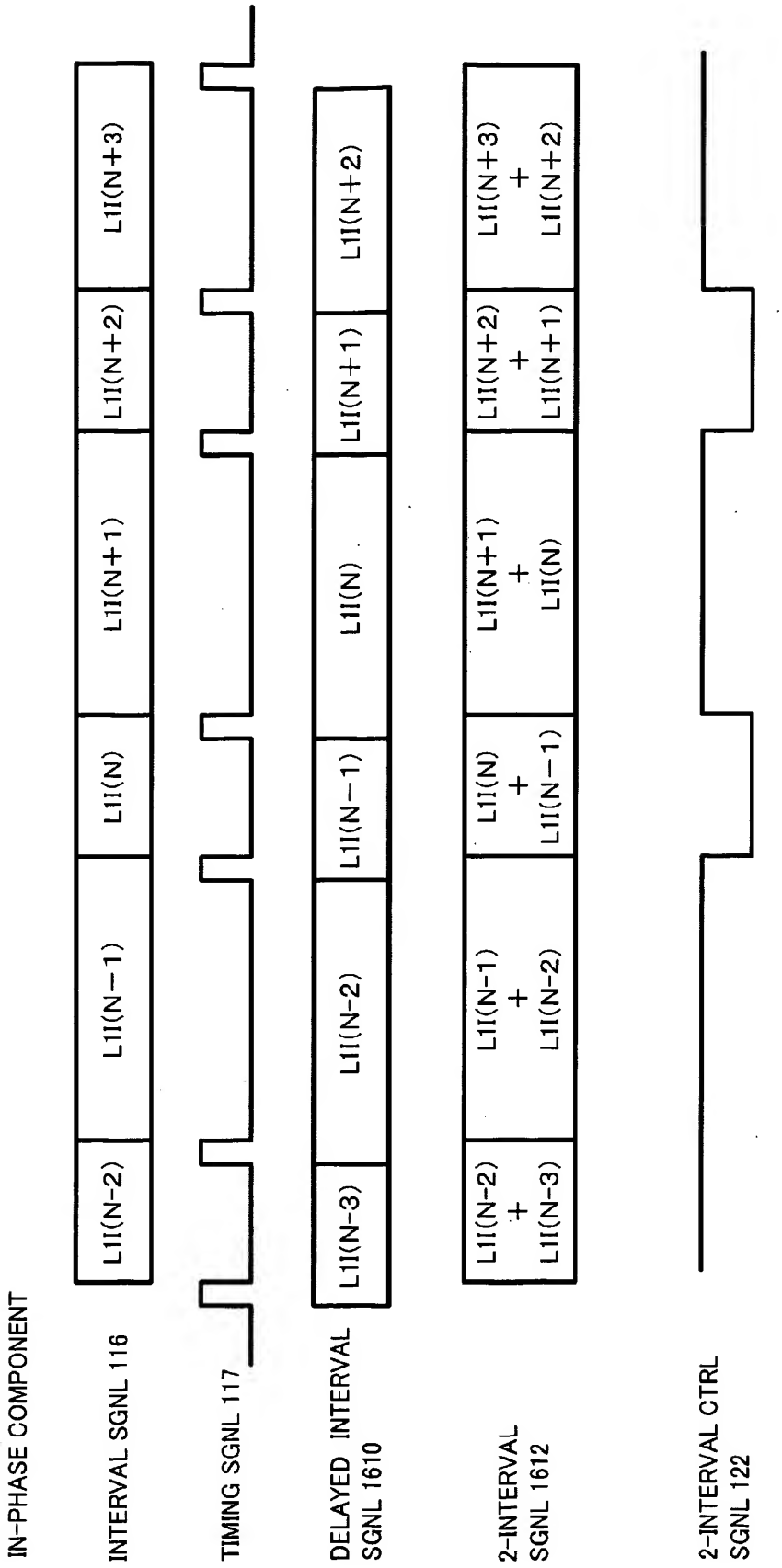

IN-PHASE COMPONENT
INTERVAL SGNL 116
L1I(N-2)
L1I(N-1)
L1I(N)
L1I(N+1)
L1I(N+2)
L1I(N+3)
TIMING SGNL 117
DELAYED INTERVAL SGNL 1610
L1I(N-3)
L1I(N-2)
L1I(N-1)
L1I(N)
L1I(N+1)
L1I(N+2)
2-INTERVAL SGNL 1612
L1I(N-2) + L1I(N-3)
L1I(N-1) + L1I(N-2)
L1I(N) + L1I(N-1)
L1I(N+1) + L1I(N)
L1I(N+2) + L1I(N+1)
L1I(N+3) + L1I(N+2)
2-INTERVAL CTRL SGNL 122

FIG.18

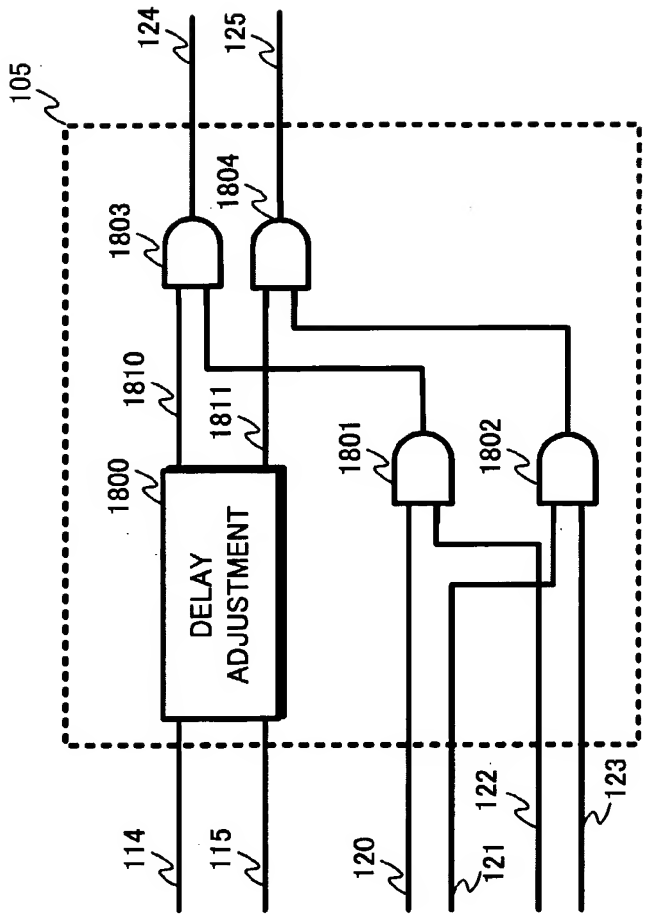

105
124
125
1803
1804
1810
1811
1800
1801
1802
DELAY ADJUSTMENT
114
115
120
121
122
123

FIG.19

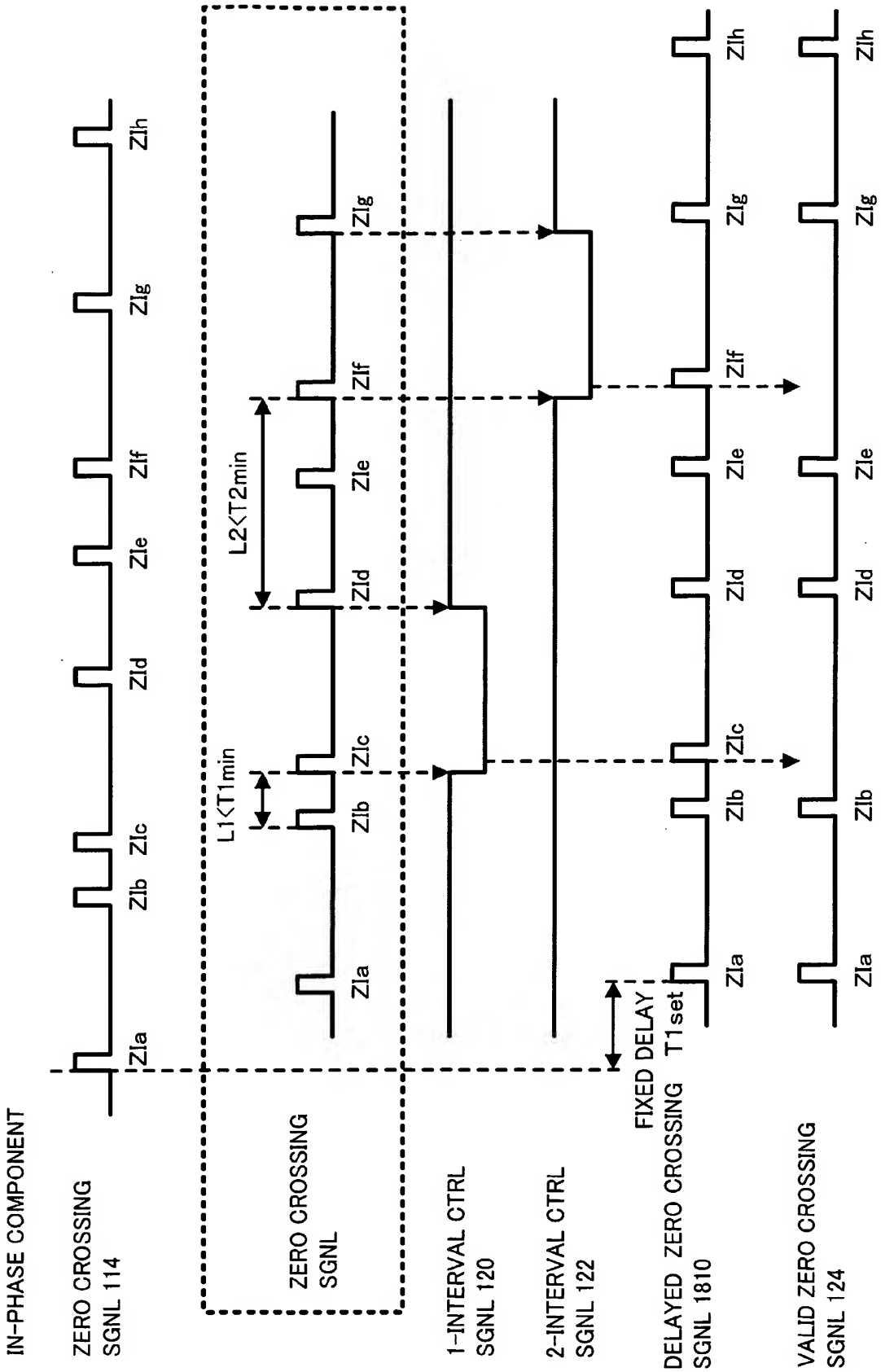

IN-PHASE COMPONENT
ZERO CROSSING SGNL 114
ZIa
ZIb
ZIc
ZId
ZIe
ZIf
ZIg
ZIh
L1<T1min
L2<T2min
ZERO CROSSING SGNL
1-INTERVAL CTRL SGNL 120
2-INTERVAL CTRL SGNL 122
FIXED DELAY T1set
DELAYED ZERO CROSSING SGNL 1810
VALID ZERO CROSSING SGNL 124

FIG.20A

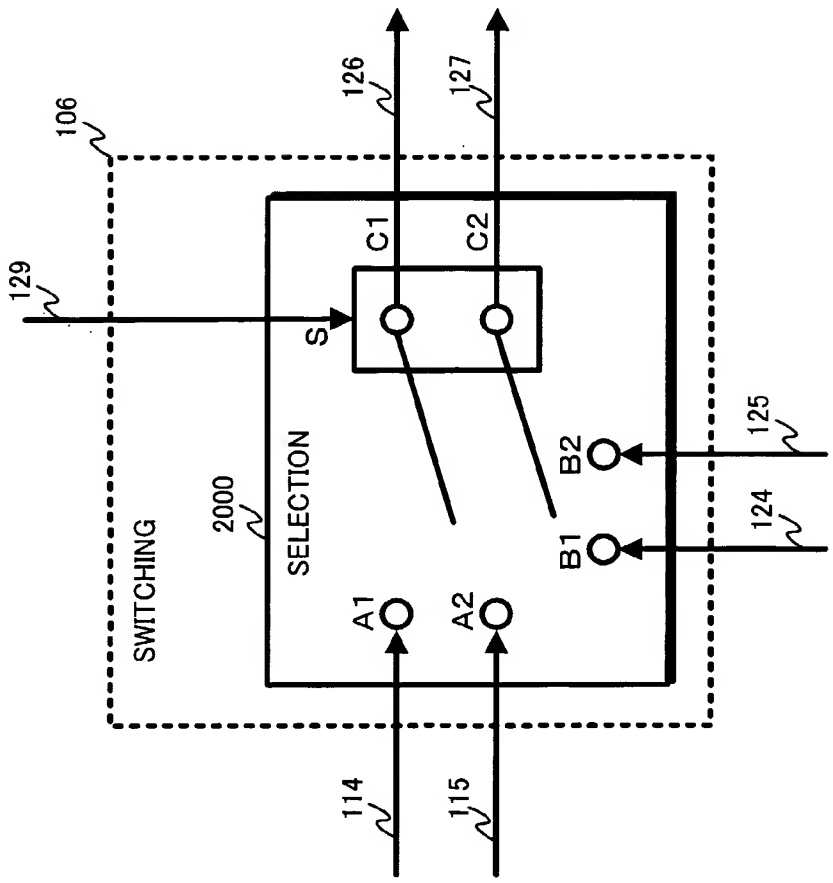


FIG.20B

TRUTH TABLE

CONTROL SIGNAL S	OUTPUT (C1, C2)
0	(B1, B2)
1	(A1, A2)

FIG.21

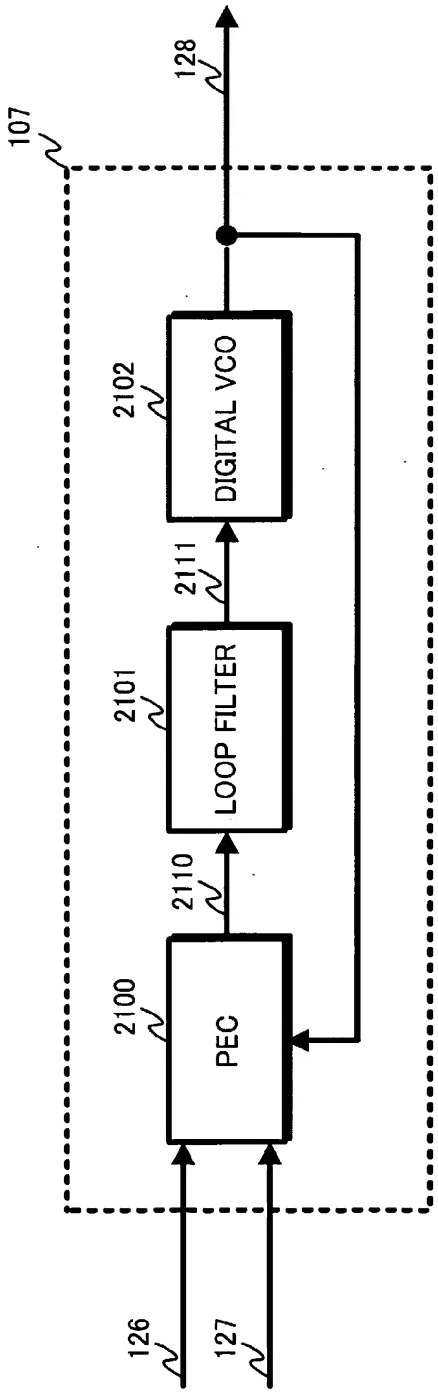

107
128
2102
DIGITAL VCO
2111
2101
LOOP FILTER
2110
2100
PEC
126
127

FIG.22

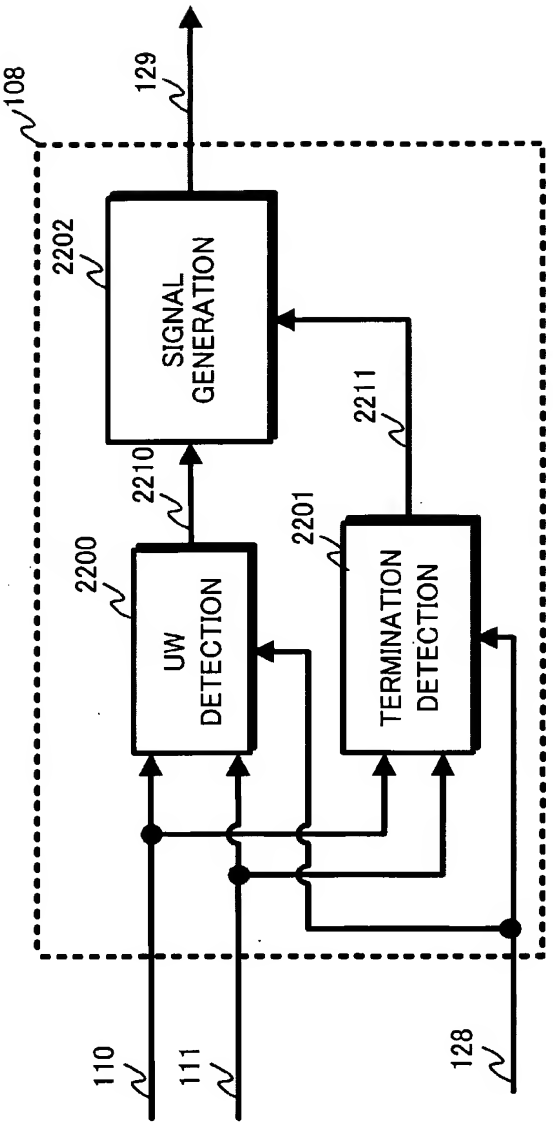

108
129
2202
SIGNAL GENERATION
2211
2210
2201
2200
UW DETECTION
TERMINATION DETECTION
110
111
128

FIG.23

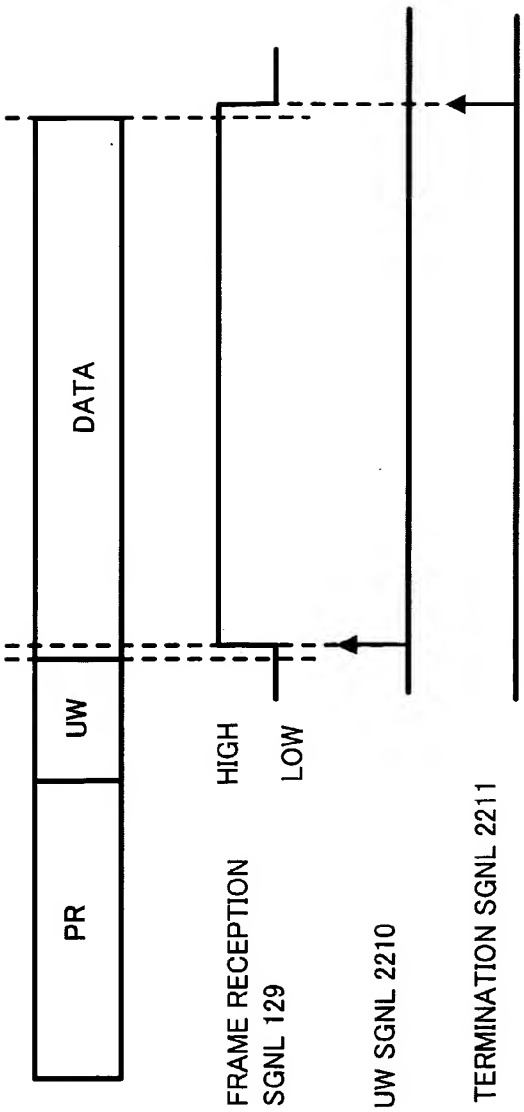

PR
UW
DATA
HIGH
LOW
FRAME RECEPTION SGNL 129
UW SGNL 2210
TERMINATION SGNL 2211

FIG.24

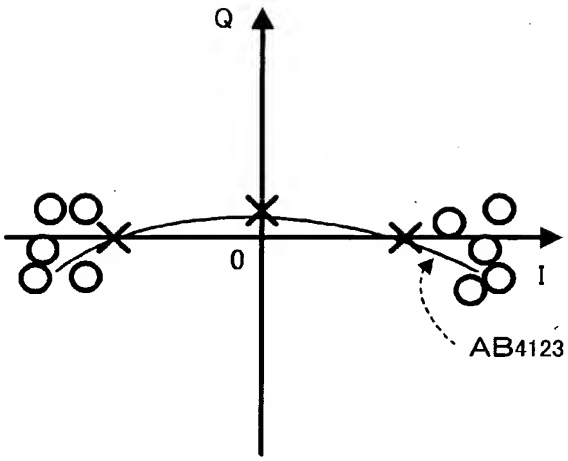


FIG.25

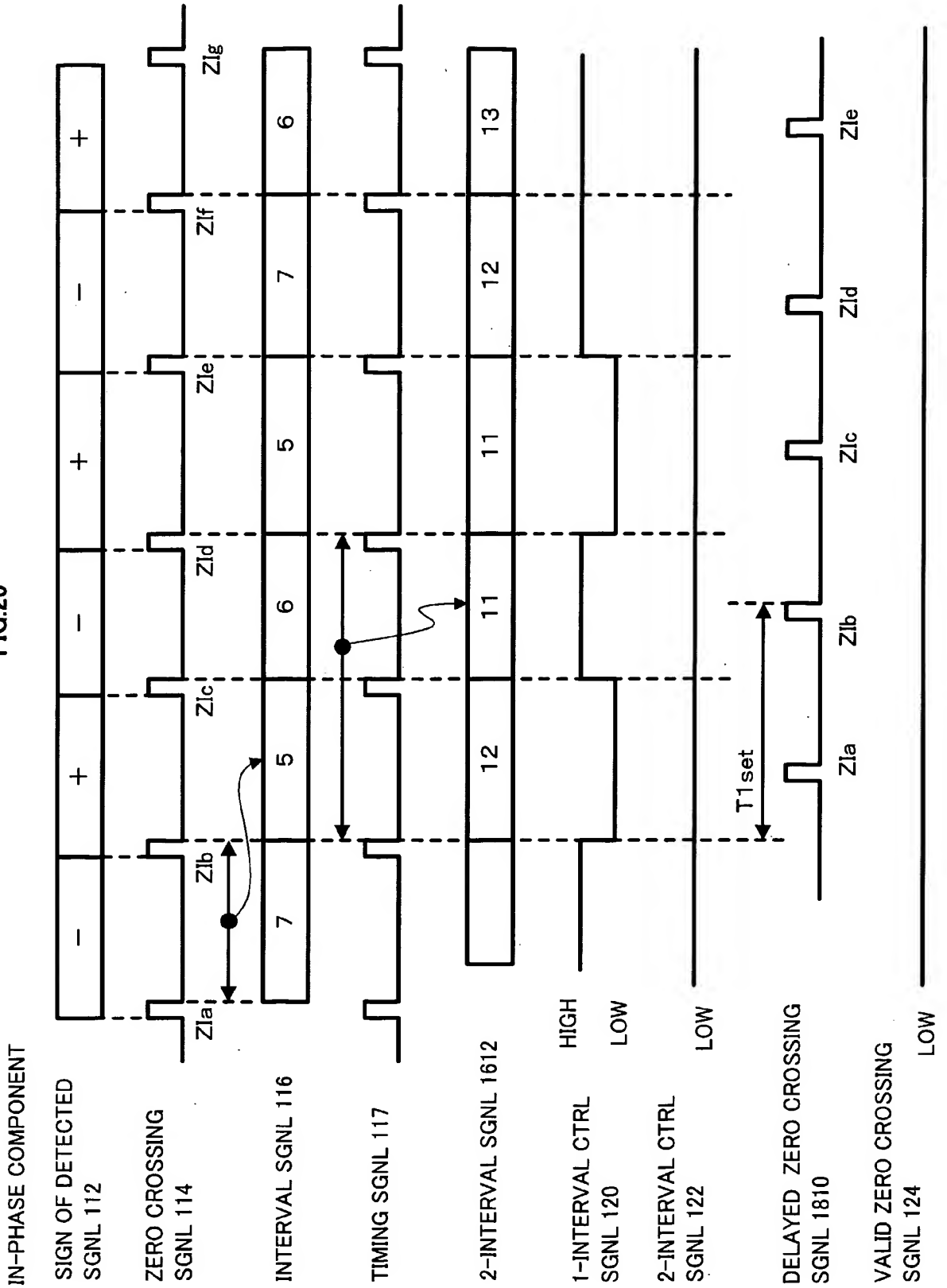
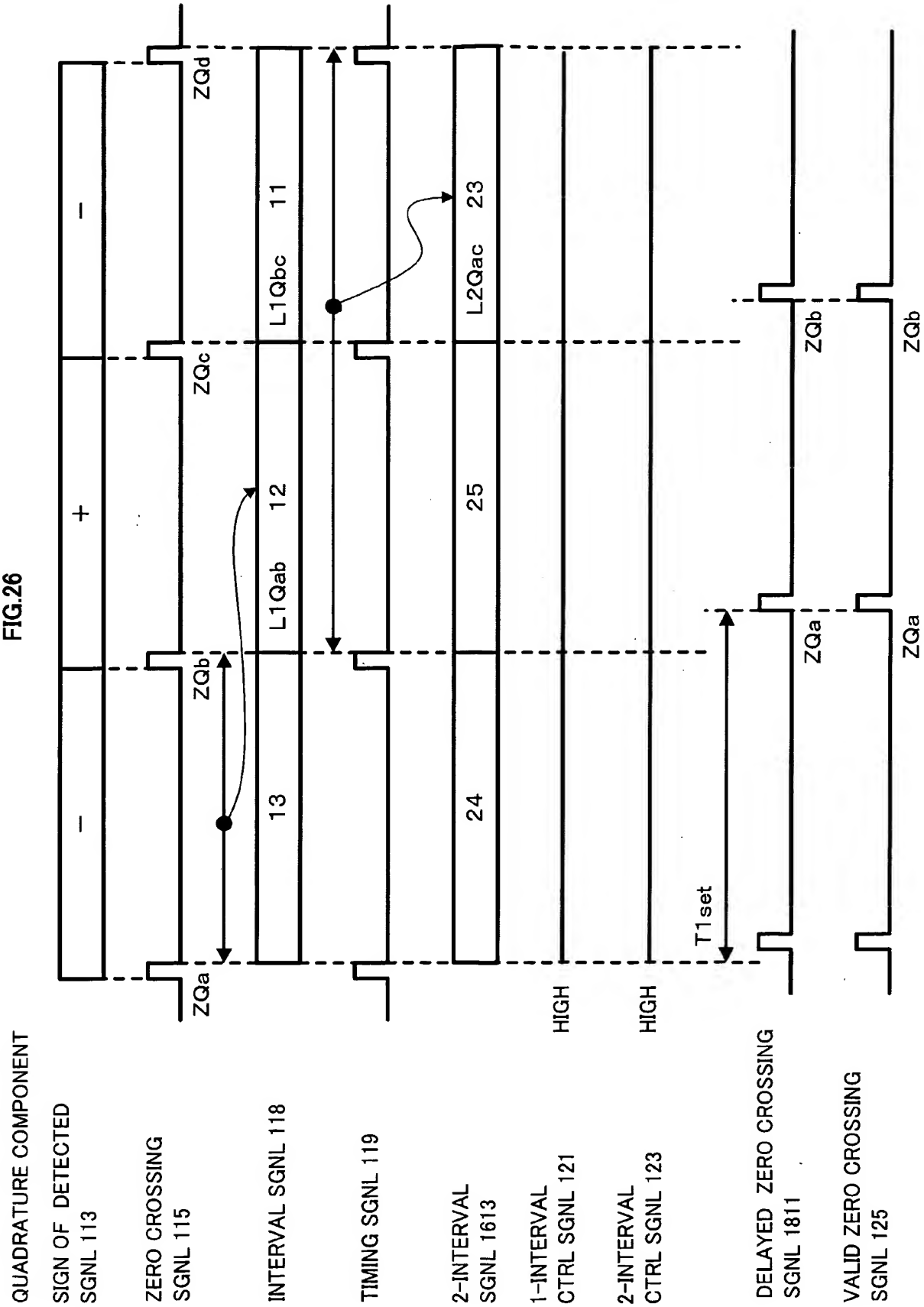

IN-PHASE COMPONENT
SIGN OF DETECTED SGNL 112
ZERO CROSSING SGNL 114
INTERVAL SGNL 116
TIMING SGNL 117
2-INTERVAL SGNL 1612
1-INTERVAL CTRL SGNL 120
2-INTERVAL CTRL SGNL 122
DELAYED ZERO CROSSING SGNL 1810
VALID ZERO CROSSING SGNL 124
HIGH
LOW
LOW
LOW
Zla
Zlb
Zlc
Zld
Zle
Zlf
Zlg
T1set
12
11
13
7
6
5

FIG.26


QUADRATURE COMPONENT
SIGN OF DETECTED SGNL 113
ZERO CROSSING SGNL 115
INTERVAL SGNL 118
TIMING SGNL 119
2-INTERVAL SGNL 1613
1-INTERVAL CTRL SGNL 121
2-INTERVAL CTRL SGNL 123
DELAYED ZERO CROSSING SGNL 1811
VALID ZERO CROSSING SGNL 125
+
−
−
ZQa
ZQb
ZQc
ZQd
13
L1Qab 12
L1Qbc 11
24
25
L2Qac 23
HIGH
HIGH
T1set
ZQa
ZQb
ZQa
ZQb

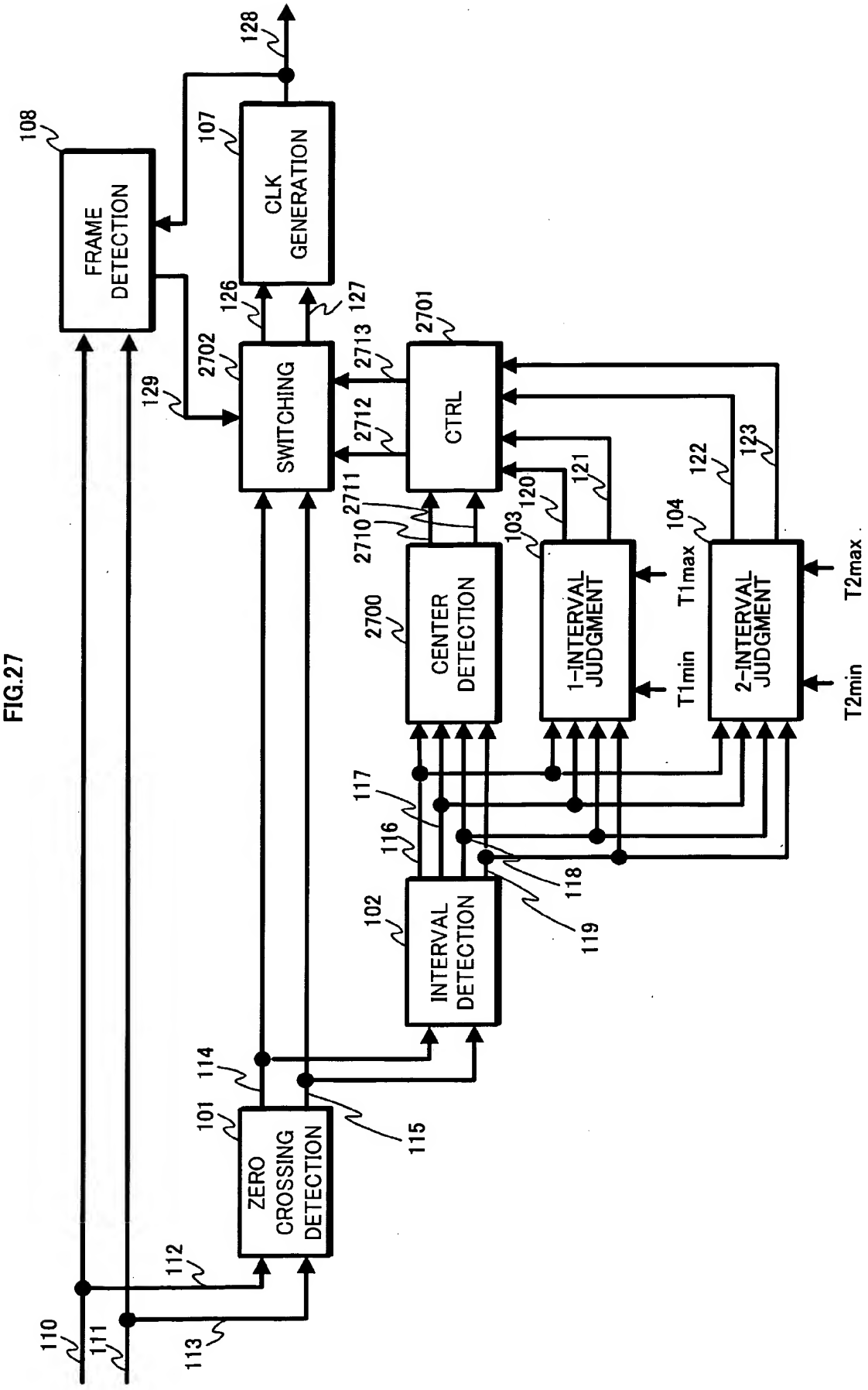

FRAME DETECTION
CLK GENERATION
SWITCHING
CTRL
CENTER DETECTION
1-INTERVAL JUDGMENT
2-INTERVAL JUDGMENT
INTERVAL DETECTION
ZERO CROSSING DETECTION
T1min
T1max
T2min
T2max
108
107
128
126
127
2702
2713
2701
129
2712
2711
2710
2700
103
120
121
104
122
123
117
116
118
119
102
114
101
115
112
110
111
113

FIG.27

FIG.28

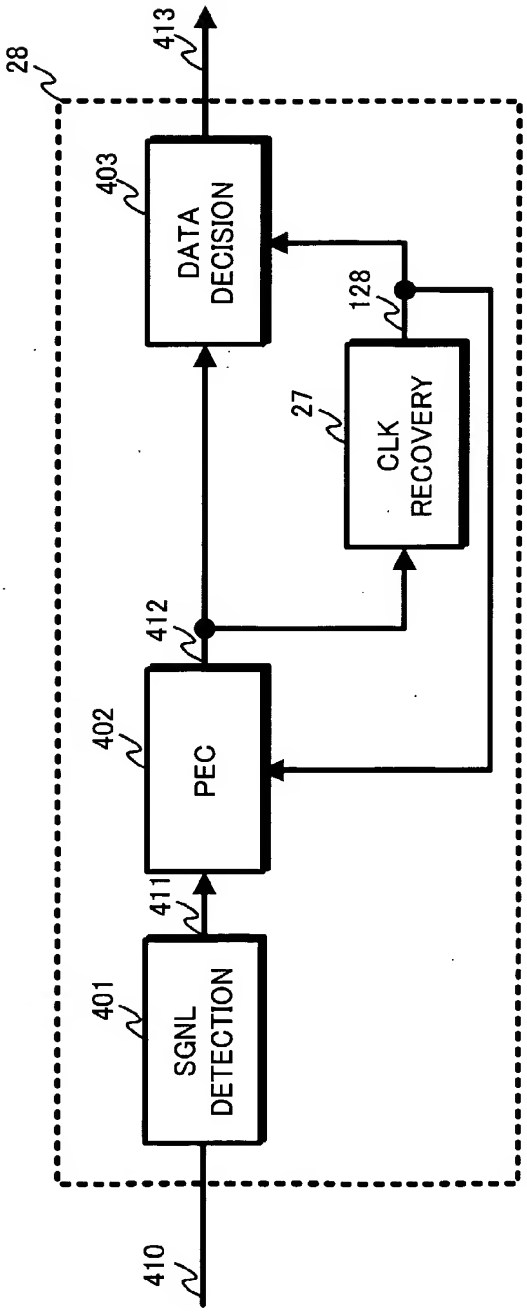

28
413
403
DATA DECISION
128
27
CLK RECOVERY
412
402
PEC
411
401
SGNL DETECTION
410

FIG.29

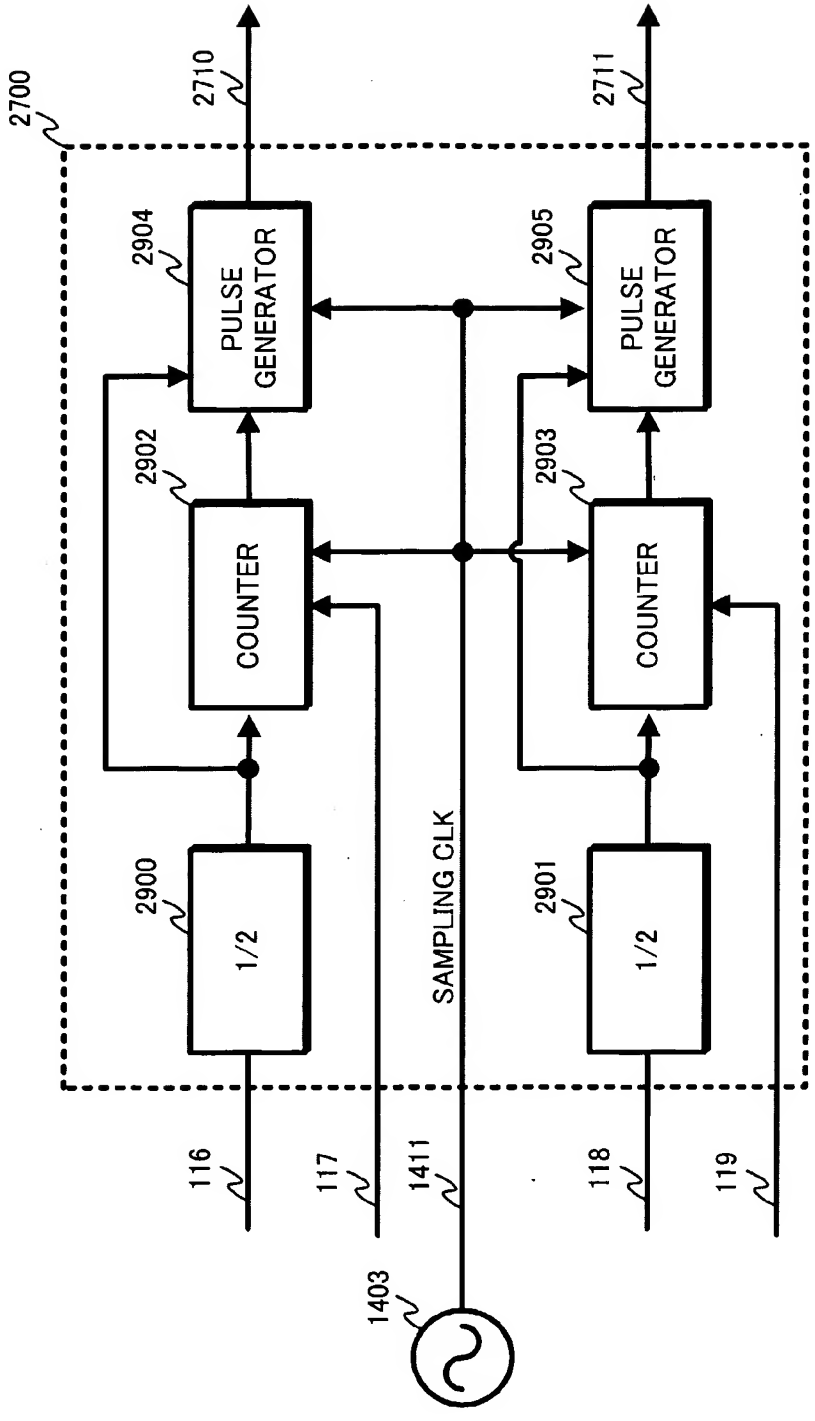

2700
2710
2711
2904
PULSE GENERATOR
2905
PULSE GENERATOR
2902
COUNTER
2903
COUNTER
2900
1/2
2901
1/2
SAMPLING CLK
116
117
1411
118
119
1403

FIG.30

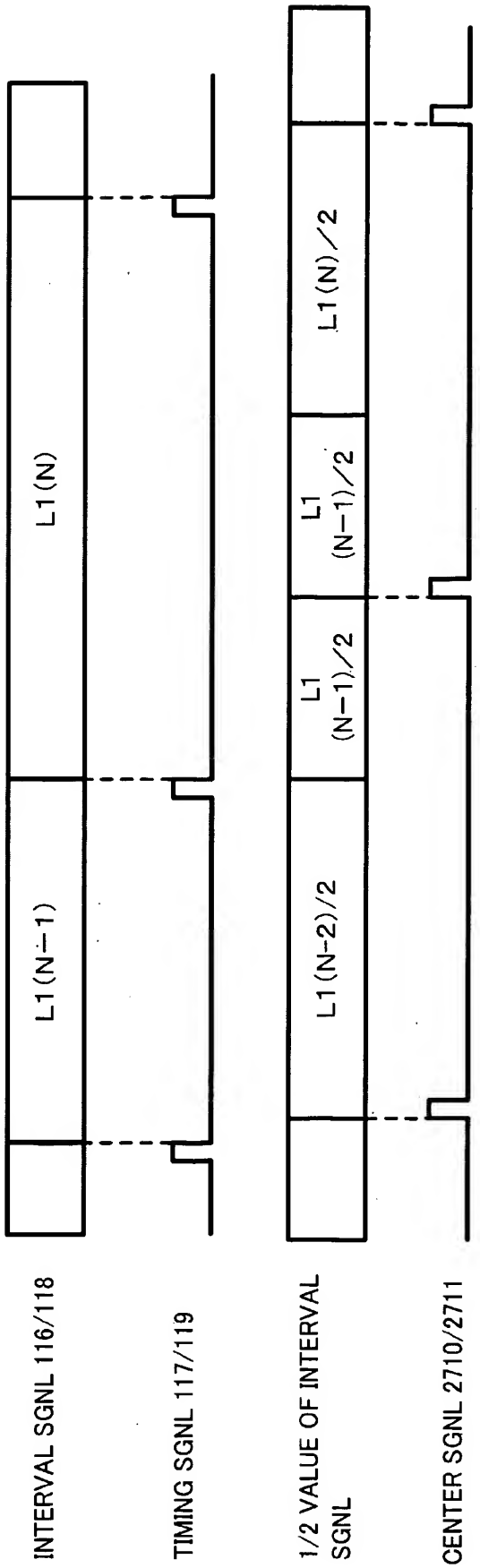

L1 (N)
L1 (N−1)
L1 (N)／2
L1 (N−1)／2
L1 (N−1)／2
L1 (N-2)／2
INTERVAL SGNL 116/118
TIMING SGNL 117/119
1/2 VALUE OF INTERVAL SGNL
CENTER SGNL 2710/2711

FIG.31

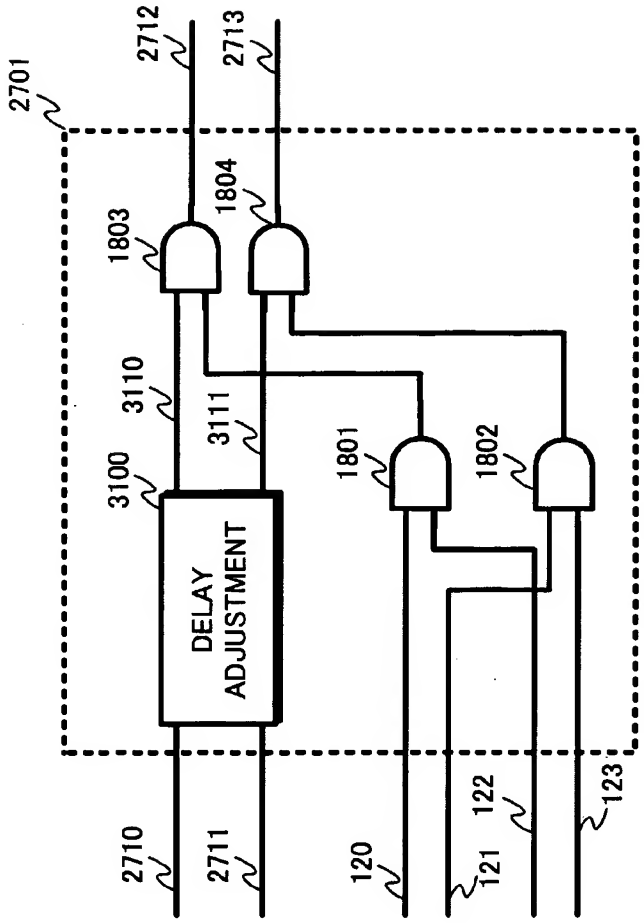

2701
2712
2713
1803
1804
3110
3111
3100
DELAY ADJUSTMENT
1801
1802
2710
2711
120
121
122
123

FIG.32

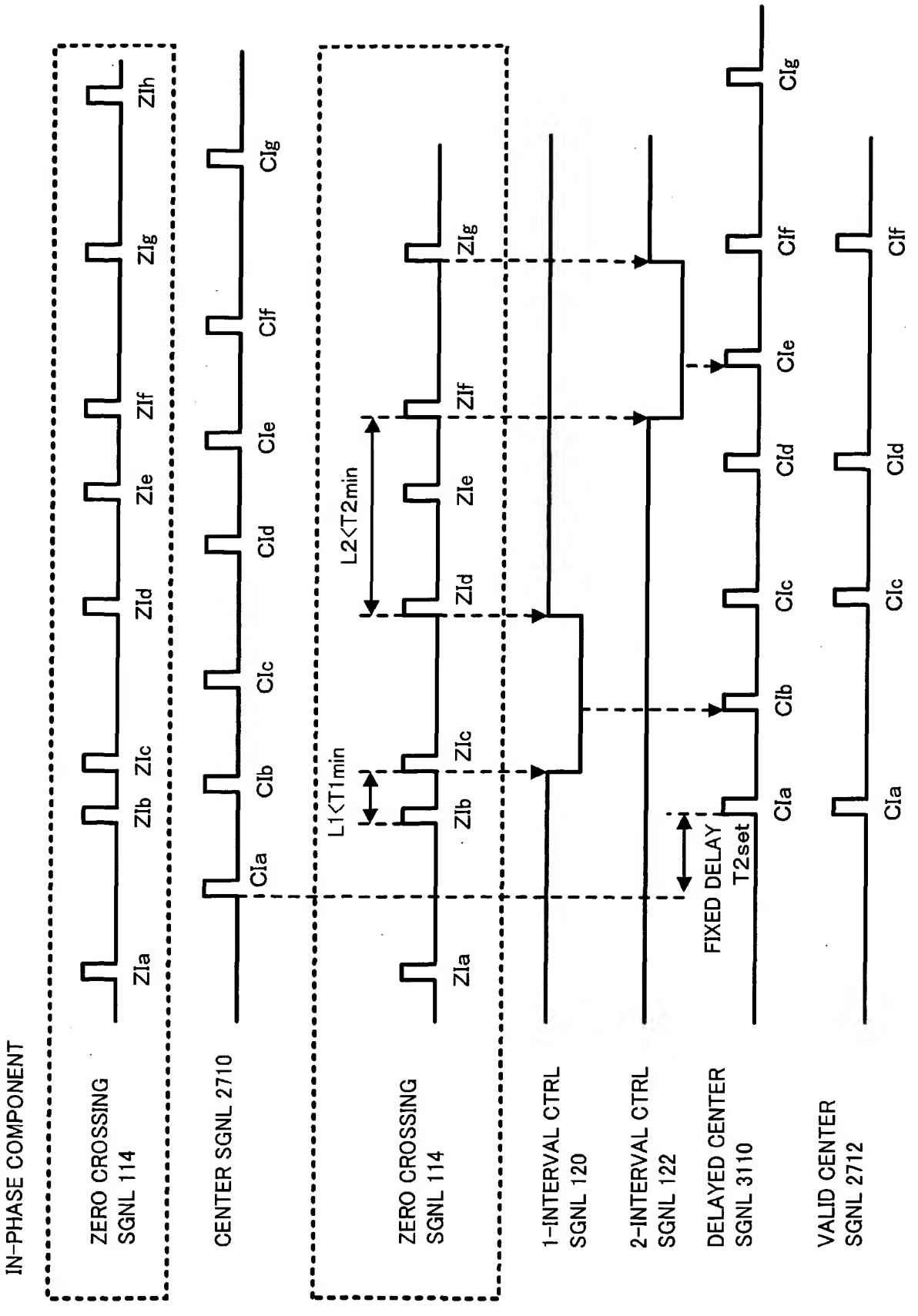

IN-PHASE COMPONENT
ZERO CROSSING SGNL 114
Zla
Zlb
Zlc
Zld
Zle
Zlf
Zlg
Zlh
CENTER SGNL 2710
Cla
Clb
Clc
Cld
Cle
Clf
Clg
L1<T1min
L2<T2min
ZERO CROSSING SGNL 114
1-INTERVAL CTRL SGNL 120
2-INTERVAL CTRL SGNL 122
FIXED DELAY T2set
DELAYED CENTER SGNL 3110
VALID CENTER SGNL 2712

FIG.33

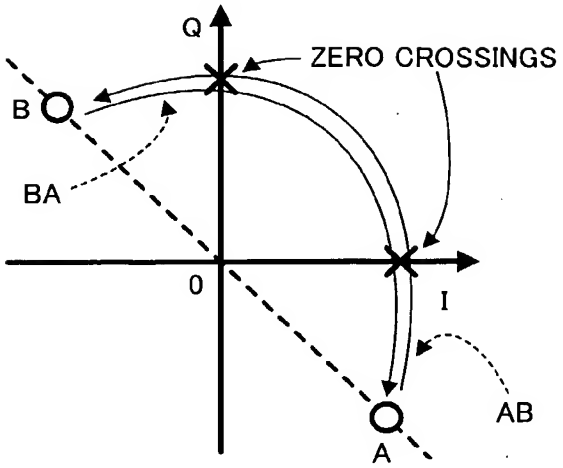


FIG.34

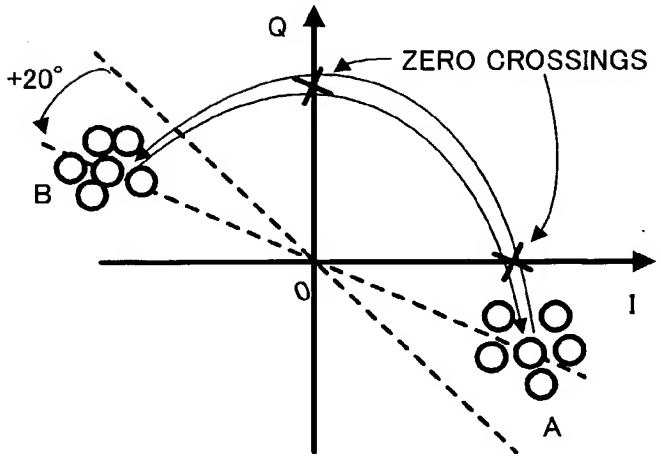


FIG.35

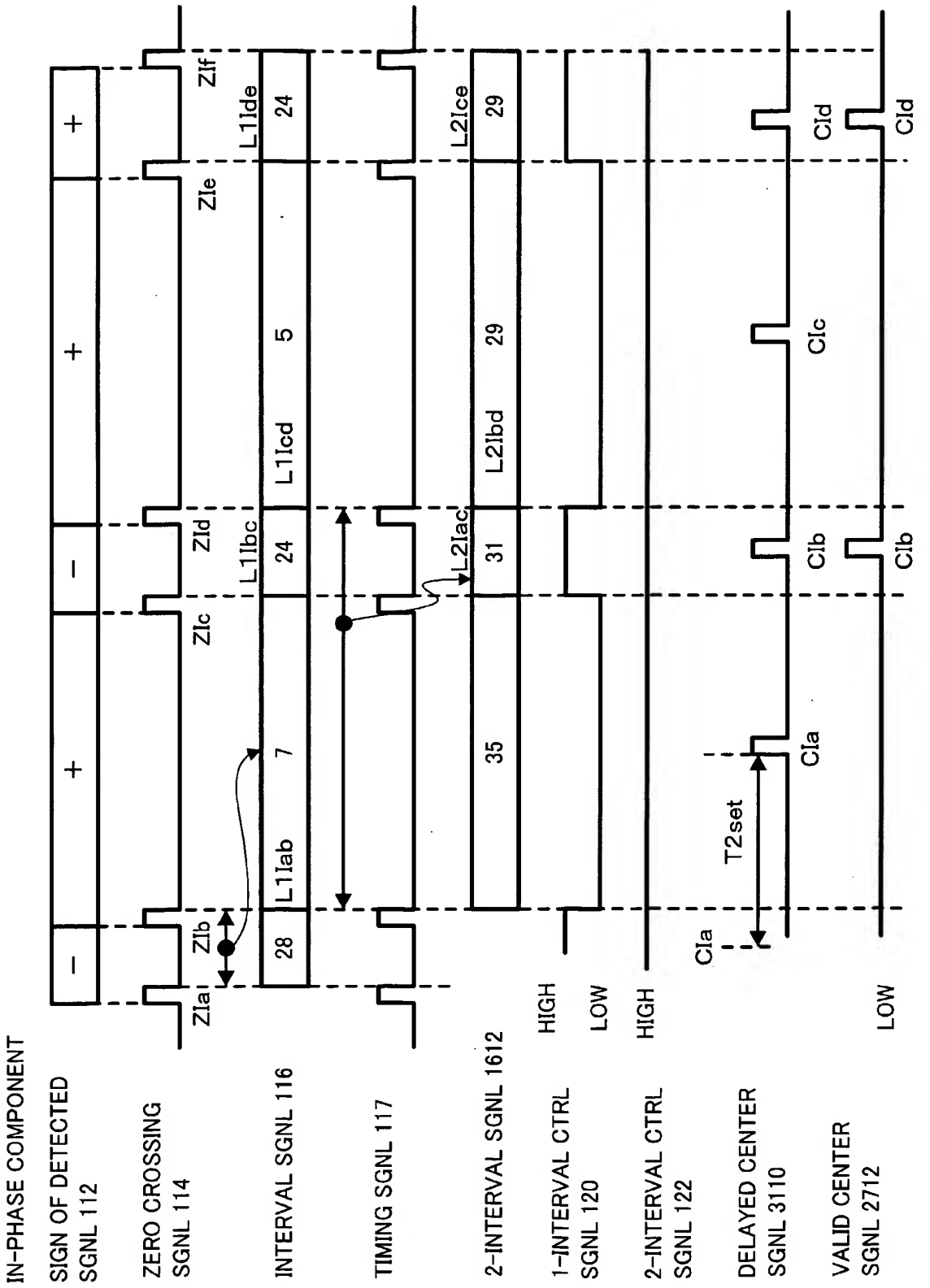

IN-PHASE COMPONENT
SIGN OF DETECTED SGNL 112
ZERO CROSSING SGNL 114
INTERVAL SGNL 116
TIMING SGNL 117
2-INTERVAL SGNL 1612
1-INTERVAL CTRL SGNL 120
2-INTERVAL CTRL SGNL 122
DELAYED CENTER SGNL 3110
VALID CENTER SGNL 2712
+
−
Zia
Zib
Zic
Zid
Zie
Zif
L1Iab
L1Ibc
L1Icd
L1Ide
28
7
24
5
24
L2Iac
L2Ibd
L2Ice
35
31
29
29
HIGH
LOW
HIGH
LOW
Cia
T2set
Cib
Cic
Cid

FIG.36

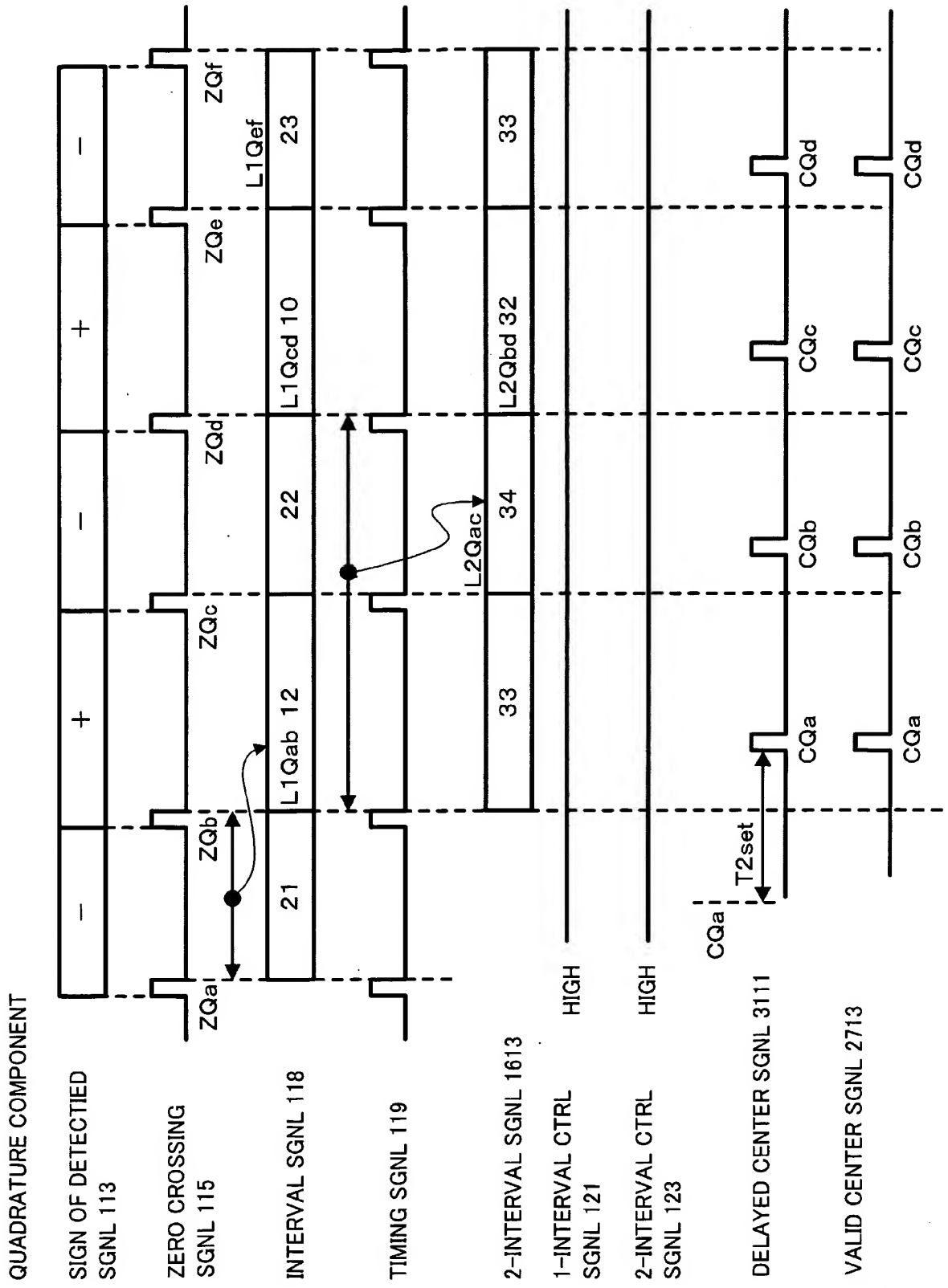

QUADRATURE COMPONENT
SIGN OF DETECTIED SGNL 113
ZERO CROSSING SGNL 115
INTERVAL SGNL 118
TIMING SGNL 119
2-INTERVAL SGNL 1613
1-INTERVAL CTRL SGNL 121
2-INTERVAL CTRL SGNL 123
DELAYED CENTER SGNL 3111
VALID CENTER SGNL 2713
ZQa
ZQb
ZQc
ZQd
ZQe
ZQf
L1Qef
L1Qab 12
L1Qcd 10
L2Qbd 32
L2Qac
21
22
23
33
34
HIGH
HIGH
CQa
CQb
CQc
CQd
T2set

FIG.37

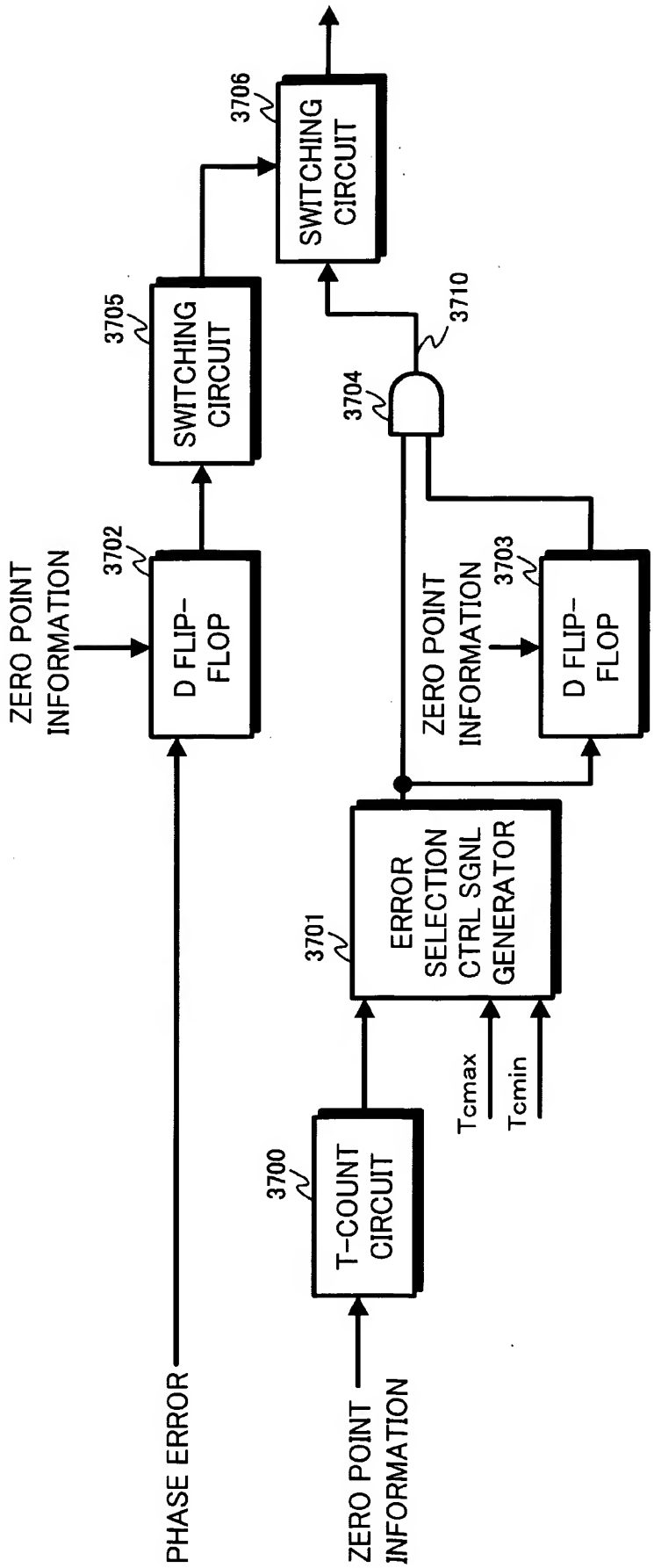

3706
SWITCHING CIRCUIT
3705
SWITCHING CIRCUIT
3710
3704
ZERO POINT INFORMATION
3702
D FLIP-FLOP
ZERO POINT INFORMATION
3703
D FLIP-FLOP
3701
ERROR SELECTION CTRL SGNL GENERATOR
Tcmax
Tcmin
3700
T-COUNT CIRCUIT
PHASE ERROR
ZERO POINT INFORMATION

FIG.39

	BIT X_n X_{n+1} X_{n+2}	PHASE TRANSITION
S1	0 0 0	$\pi/8$
S2	0 0 1	$3\pi/8$
S3	0 1 1	$5\pi/8$
S4	0 1 0	$7\pi/8$
S5	1 1 0	$-7\pi/8$
S6	1 1 1	$-5\pi/8$
S7	1 0 1	$-3\pi/8$
S8	1 0 0	$-\pi/8$

FIG.38

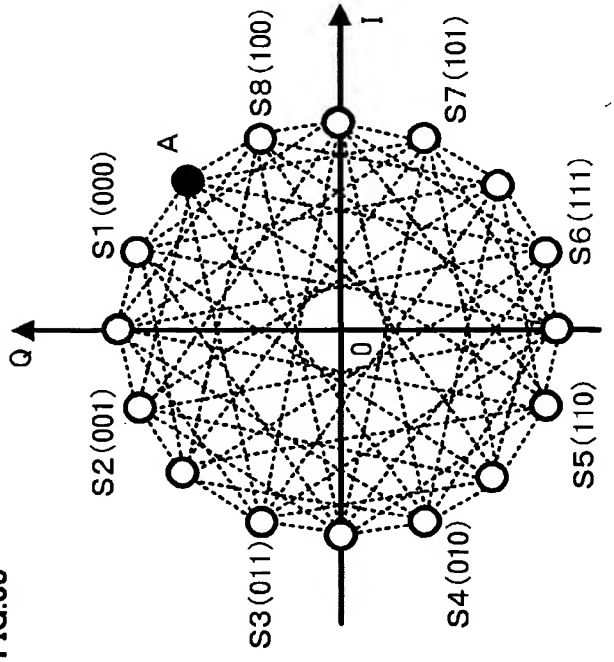
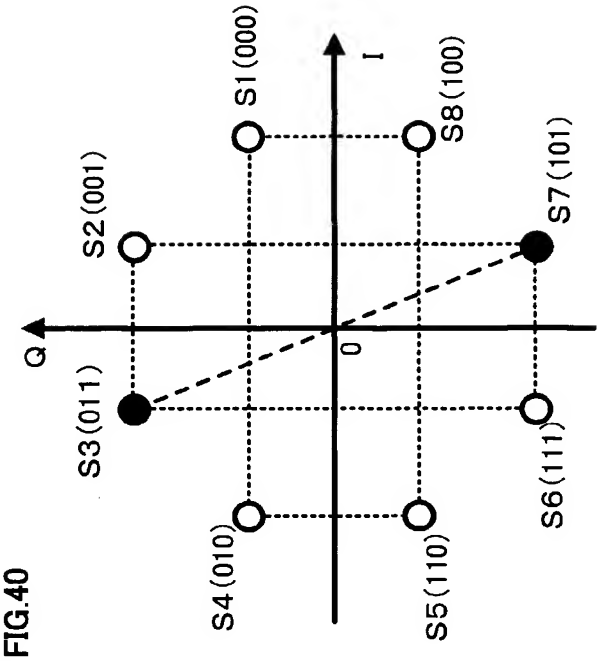


FIG.40



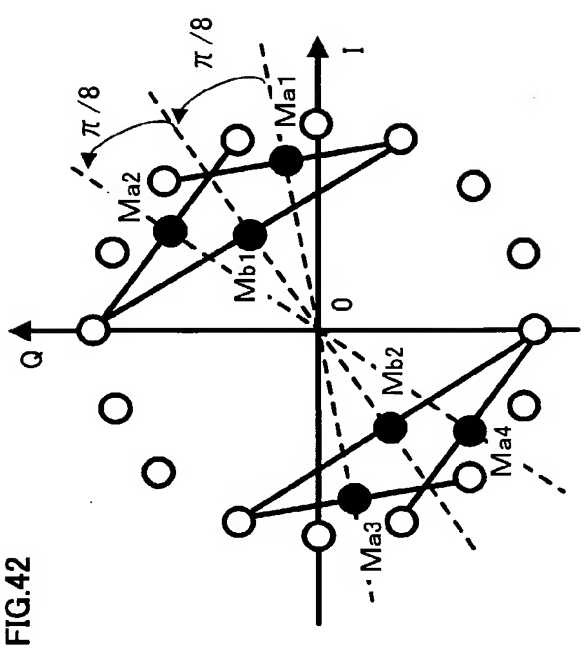


FIG.42

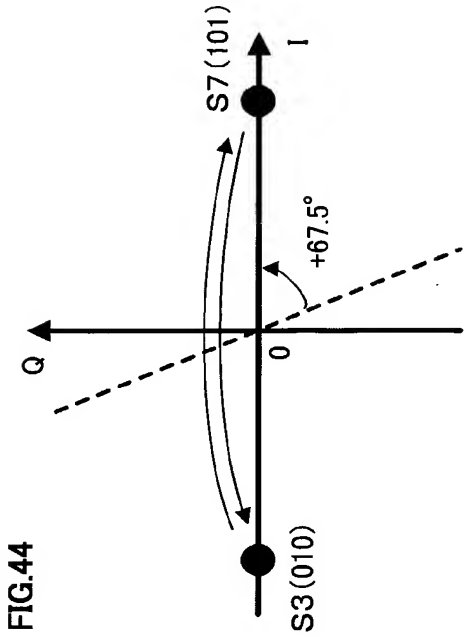


FIG.44

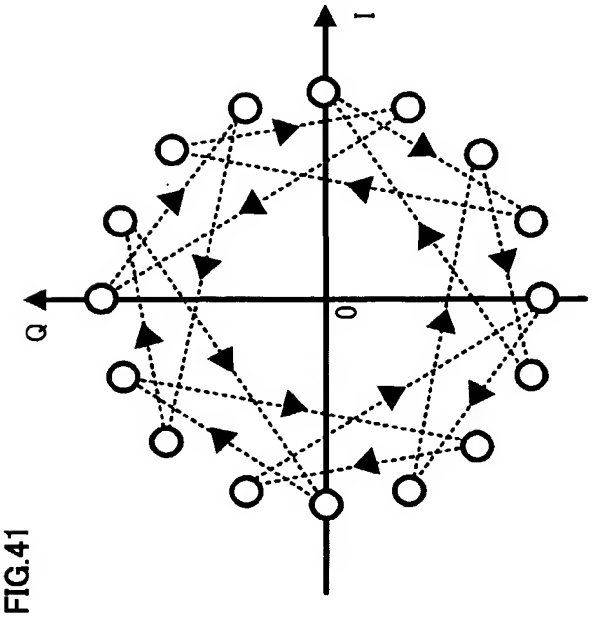


FIG.41

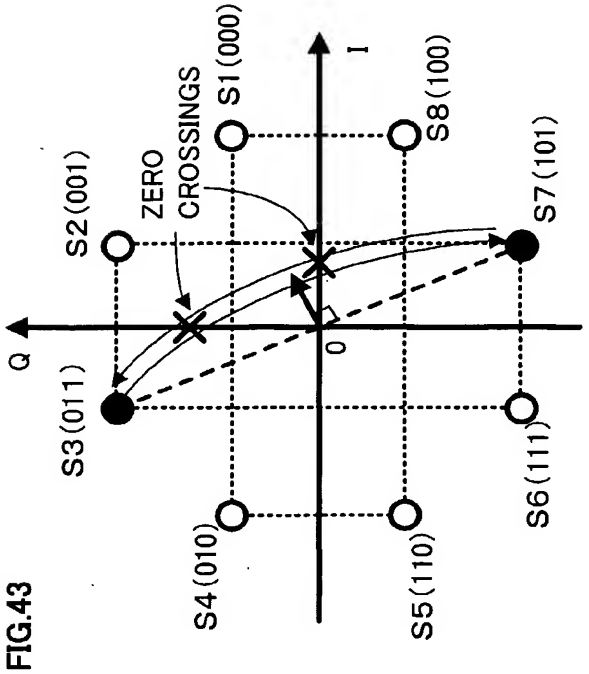


FIG.43

FIG.46

BIT X_n	PHASE TRANSITION
0	0
1	π

FIG.45

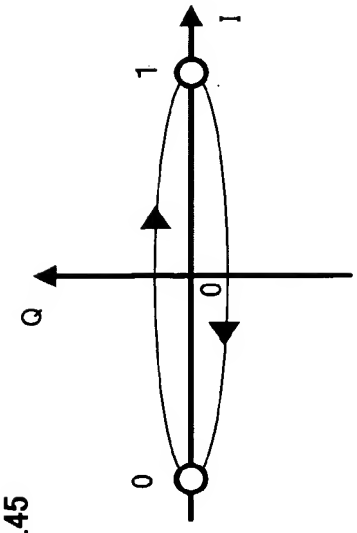


FIG.48

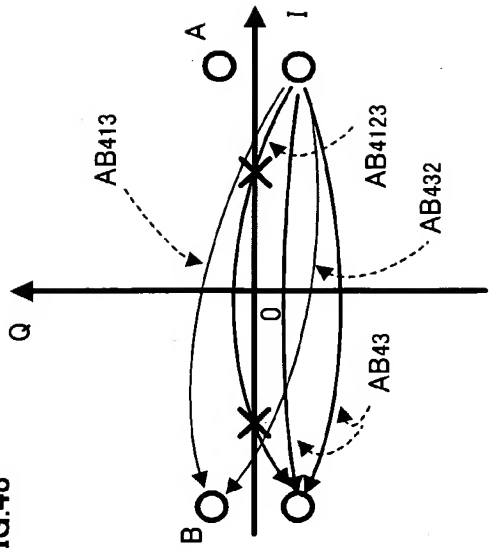


FIG.47

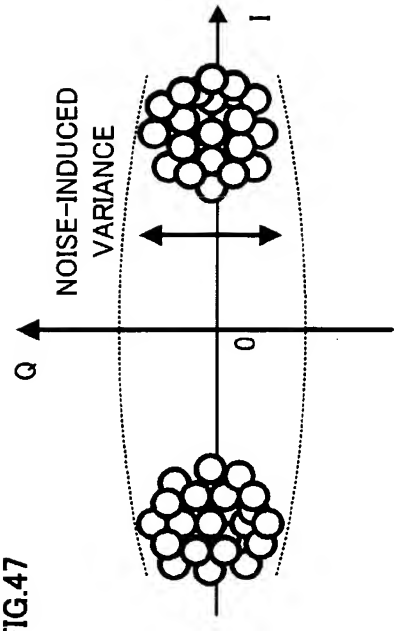


FIG.50

	BIT X_n X_{n+1}	PHASE TRANSITION
S1	0 0	$\pi/4$
S2	0 1	$3\pi/4$
S3	1 1	$-3\pi/4$
S4	1 0	$-\pi/4$

FIG.49

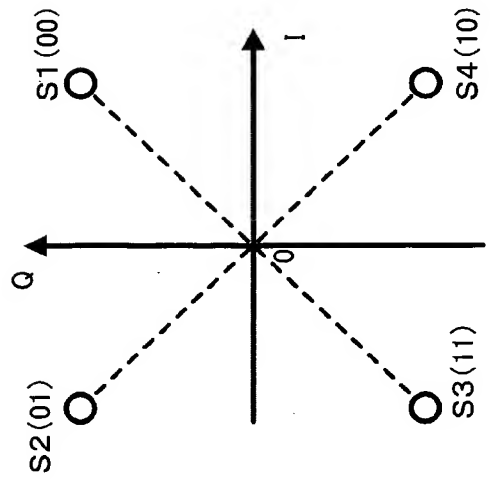


FIG.51

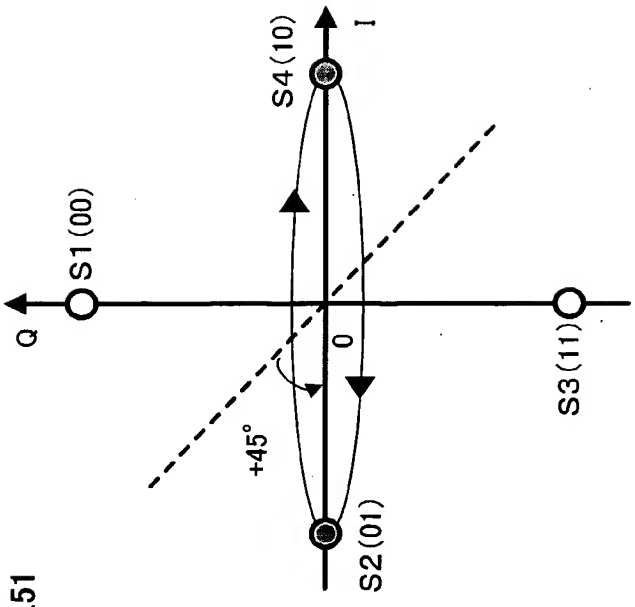


FIG.52

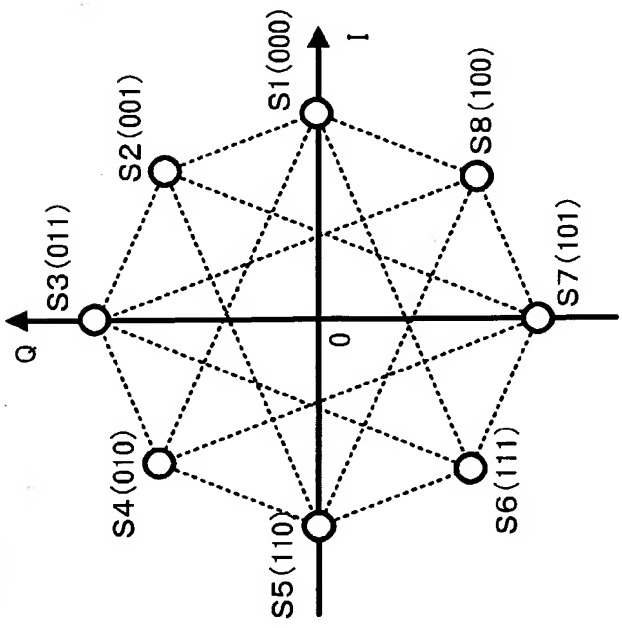


FIG.53

	BIT X_n X_{n+1} X_{n+2}	PHASE TRANSITION
S1	0 0 0	0
S2	0 0 1	$\pi/4$
S3	0 1 1	$2\pi/4$
S4	0 1 0	$3\pi/4$
S5	1 1 0	π
S6	1 1 1	$-3\pi/4$
S7	1 0 1	$-2\pi/4$
S8	1 0 0	$-\pi/4$

FIG.54